AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A flash memory cell comprising:

a substrate comprising a source and a drain;

a silicon dioxide layer ~~comprising a silicon material and adjacent~~ adjoining said substrate;

a polysilicon floating gate;

a dielectric layer sandwiched between and adjoining both ~~adjacent~~ said silicon dioxide layer and said floating gate, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide;

~~a floating gate adjacent said dielectric layer;~~

an oxide-nitride-oxide (ONO) layer adjoining ~~adjacent~~ said floating gate; and

a control gate adjoining ~~adjacent~~ said ONO layer.

2-6. (Canceled).

7. (Original) The flash memory cell of Claim 1 wherein said dielectric material comprises a metal oxide.

8. (Original) The flash memory cell of Claim 1 wherein said dielectric layer comprises a composite of a metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

9. (Canceled).

10. (Currently Amended) A flash memory array comprising memory cells, wherein a memory cell comprises:

a substrate comprising a source and a drain;

a first layer comprising a silicon material;

a tunnel oxide layer sandwiched between and adjoining both ~~adjacent~~ said substrate and said first layer, said tunnel oxide layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide;

~~a layer comprising a silicon material and adjacent said tunnel oxide layer;~~

a polysilicon floating gate adjoining ~~adjacent~~ said first ~~dielectric~~ layer;

an oxide-nitride-oxide (ONO) layer adjoining ~~adjacent~~ said floating gate; and

a control gate adjoining ~~adjacent~~ said ONO layer.

11. (Canceled).

12. (Previously Presented) The flash memory array of Claim 10 wherein said silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

13. (Previously Presented) The flash memory array of Claim 10 wherein said dielectric material comprises a metal oxide.

14-20. (Canceled).

21. (Currently Amended) A flash memory cell comprising:

a substrate comprising a source and a drain;

a first layer comprising a first silicon material and adjoining ~~adjacent~~ said

substrate;

a second layer comprising a second silicon material;

a dielectric layer sandwiched between and adjoining both ~~adjacent~~ said first ~~silicon dioxide~~ layer and said second layer, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide;

~~a second layer comprising a first silicon material and adjacent said dielectric layer;~~

a polysilicon floating gate adjoining ~~adjacent~~ said second layer ~~silicon dioxide~~;

an oxide-nitride-oxide (ONO) layer adjoining ~~adjacent~~ said floating gate; and

a control gate adjoining ~~adjacent~~ said ONO layer.

22. (Original) The flash memory cell of Claim 21 wherein said first silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

23. (Original) The flash memory cell of Claim 21 wherein said second silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

24. (Original) The flash memory cell of Claim 21 wherein said dielectric material comprises a metal oxide.

25. (Original) The flash memory cell of Claim 21 wherein said dielectric layer comprises a composite of a metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.